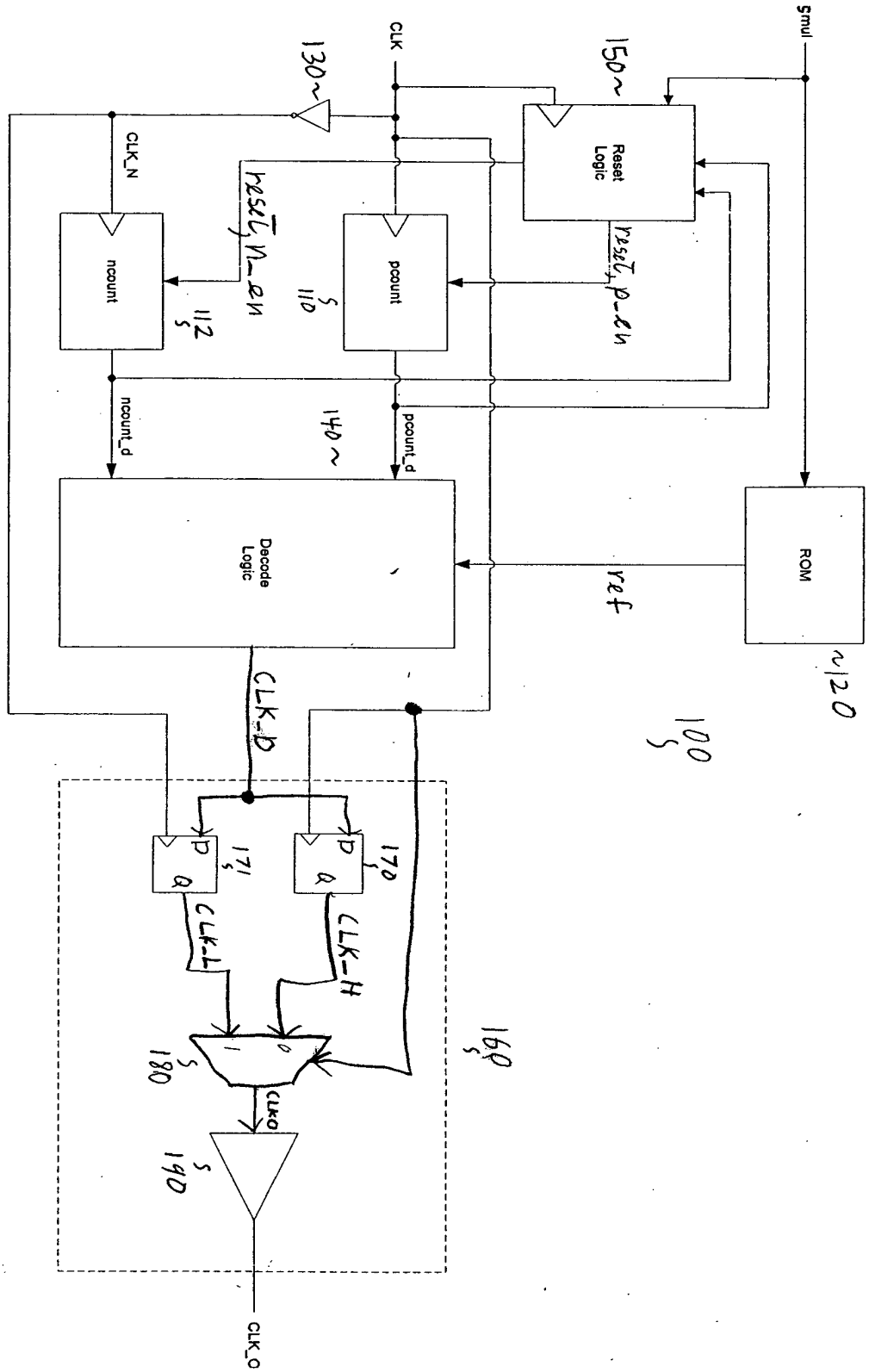
Smul
CLK
130
150
Reset Logic
reset_pcnt
reset_main
CLK_N
ncount
pcount
112
110
ncount_d
pcount_d
140
Decode Logic
ref
ROM
120
100
CLK_D
170
171
CLK_L
CLK_H
180
CLKO
190
160
CLK_O

FIG. 1

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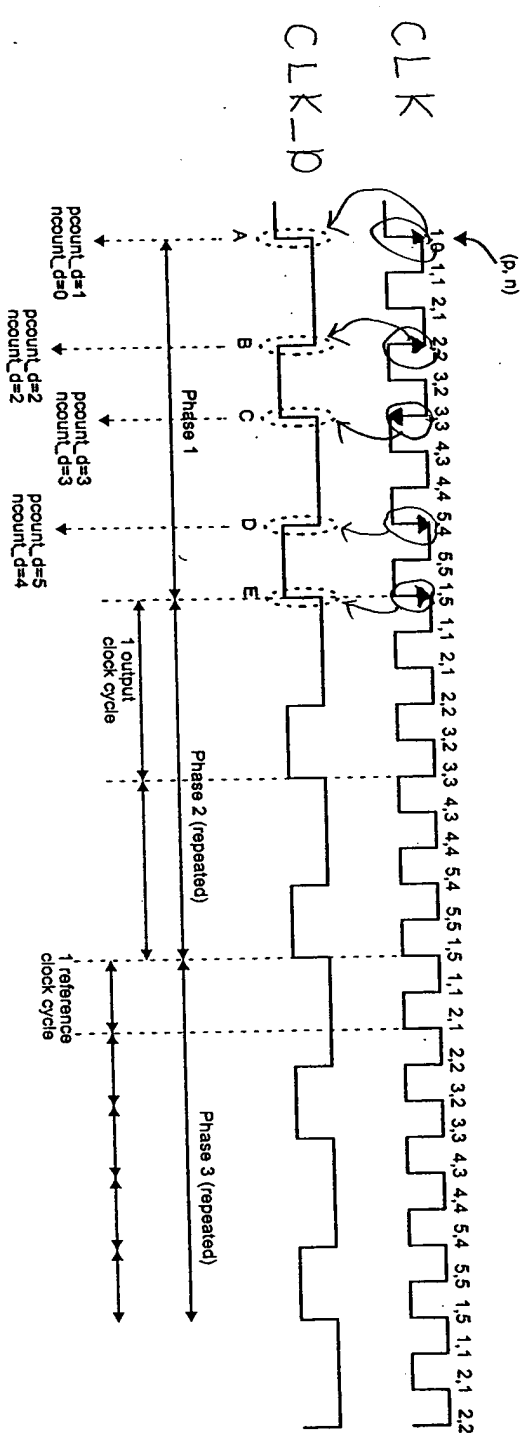
CLK
CLK_D
(p, n)
1,0 1,1 2,1 2,2 3,2 3,3 4,3 4,4 5,4 5,5 1,5 1,1 2,1 2,2 3,2 3,3 4,3 4,4 5,4 5,5 1,5 1,1 2,1 2,2 3,2 3,3 4,3 4,4 5,4 5,5 1,5 1,1 2,1 2,2
A
B
C
D
E
pcount_d=1
ncount_d=0
pcount_d=2
ncount_d=2
pcount_d=3
ncount_d=3
pcount_d=5
ncount_d=4
Phase 1
1 output clock cycle
Phase 2 (repeated)
1 reference clock cycle
Phase 3 (repeated)

FIG 2A

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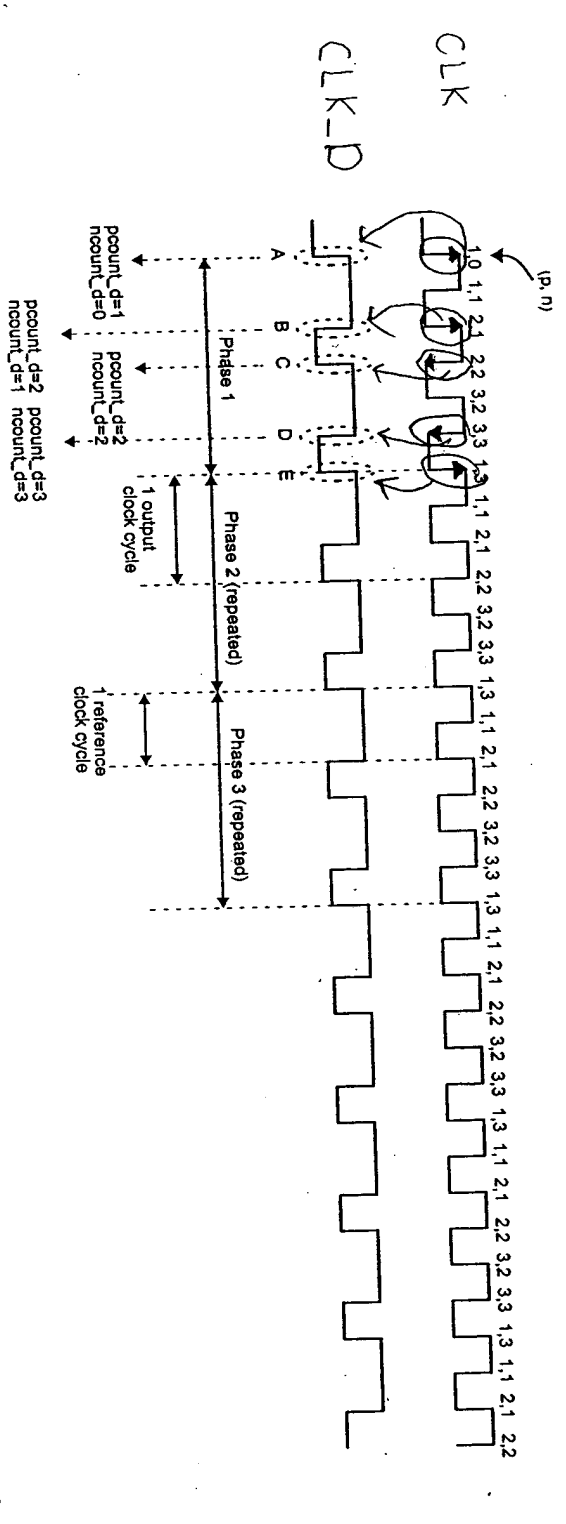
CLK
CLK_D
(p, n)
1,0 1,1 2,1 2,2 3,2 3,3 1,3 1,1 2,1 2,2 3,2 3,3 1,3 1,1 2,1 2,2 3,2 3,3 1,3 1,1 2,1 2,2 3,2 3,3 1,3 1,1 2,1 2,2
A
B
C
D
E
Phase 1
Phase 2 (repeated)
Phase 3 (repeated)
1 output clock cycle
1 reference clock cycle
pcount_d=1 ncount_d=0
pcount_d=2 ncount_d=1
pcount_d=2 ncount_d=2
pcount_d=3 ncount_d=3

FIG 2B

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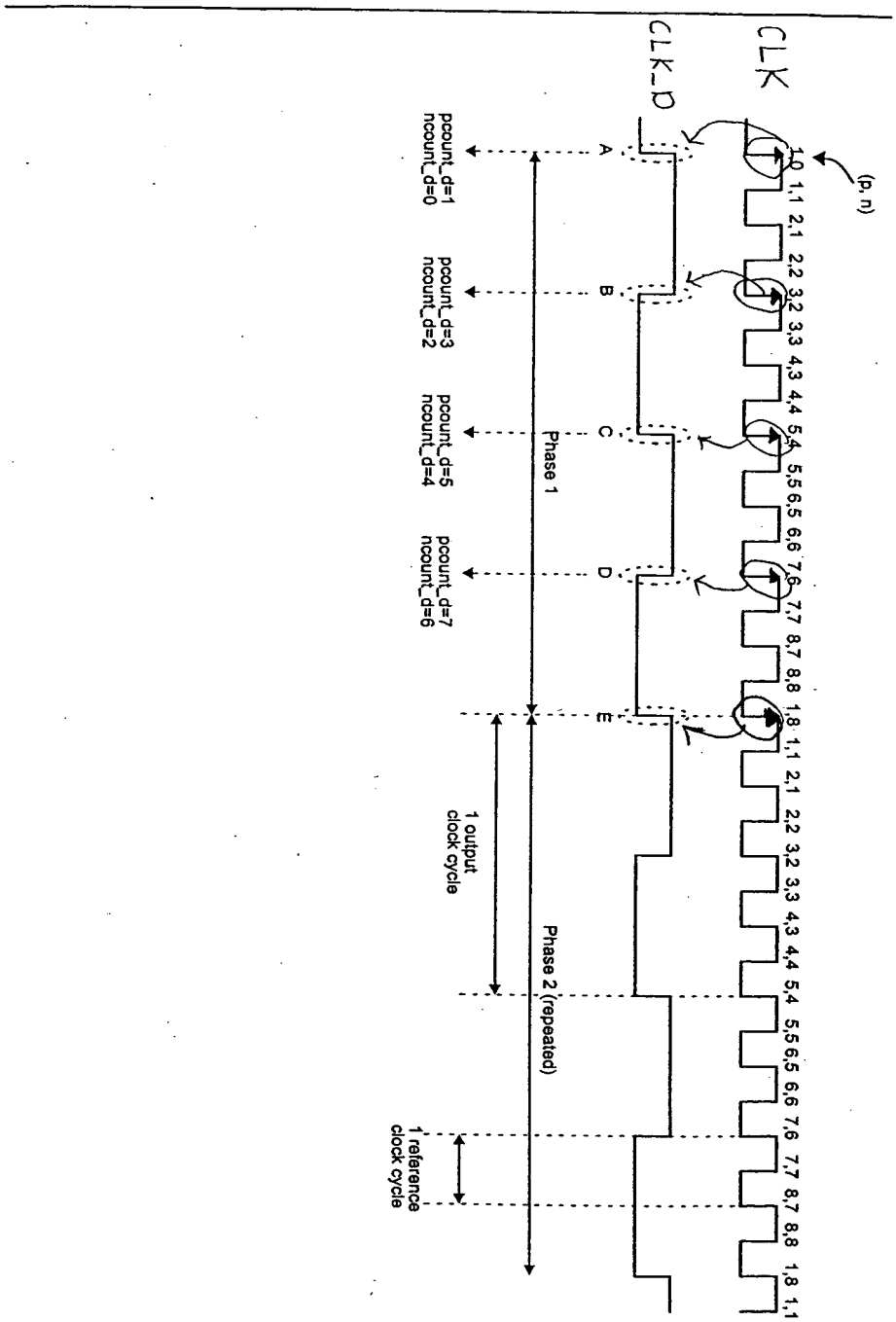
CLK
CLK_D
(p, n)
1,0 1,1 2,1 2,2 3,2 3,3 4,3 4,4 5,4 5,5 6,5 6,6 7,6 7,7 8,7 8,8 1,8 1,1 2,1 2,2 3,2 3,3 4,3 4,4 5,4 5,5 6,5 6,6 7,6 7,7 8,7 8,8 1,8 1,1
A
B
C
D
E
Phase 1
Phase 2 (repeated)
pcount_d=1 ncount_d=0
pcount_d=3 ncount_d=2
pcount_d=5 ncount_d=4
pcount_d=7 ncount_d=6
1 output clock cycle
1 reference clock cycle

FIG 2C

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	Point B		Point C		Point D	
mul (in Hex)	refhlp1	refhln1	reflhp	reflhn	refhlp2	refhln2
2	1	1	2	1	2	2
3	2	1	2	2	3	3
4	2	1	3	2	4	3
5	2	2	3	3	5	4
6	2	2	4	3	5	5
7	3	2	4	4	6	6
8	3	2	5	4	7	6
9	3	3	5	5	8	7
a	3	3	6	5	8	8
b	4	3	6	6	9	9
c	4	3	7	6	a	9
d	4	4	7	7	b	a

FIG. 3

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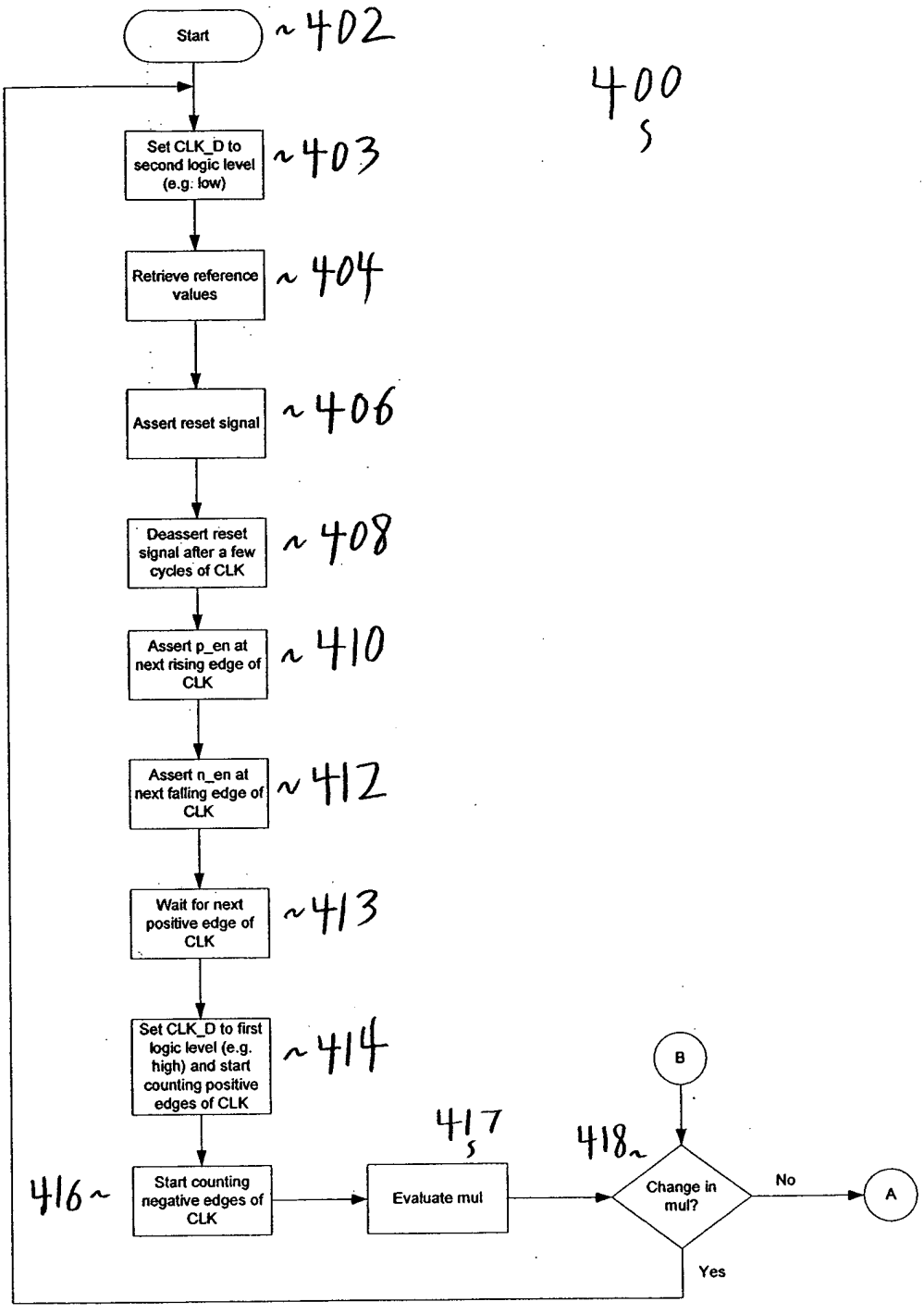
Start
402
400
Set CLK_D to second logic level (e.g. low)
403
Retrieve reference values
404
Assert reset signal
406
Deassert reset signal after a few cycles of CLK
408
Assert p_en at next rising edge of CLK
410
Assert n_en at next falling edge of CLK
412
Wait for next positive edge of CLK
413
Set CLK_D to first logic level (e.g. high) and start counting positive edges of CLK
414
416
Start counting negative edges of CLK
417
Evaluate mul
418
Change in mul?
No
Yes
B
A

FIG. 4A

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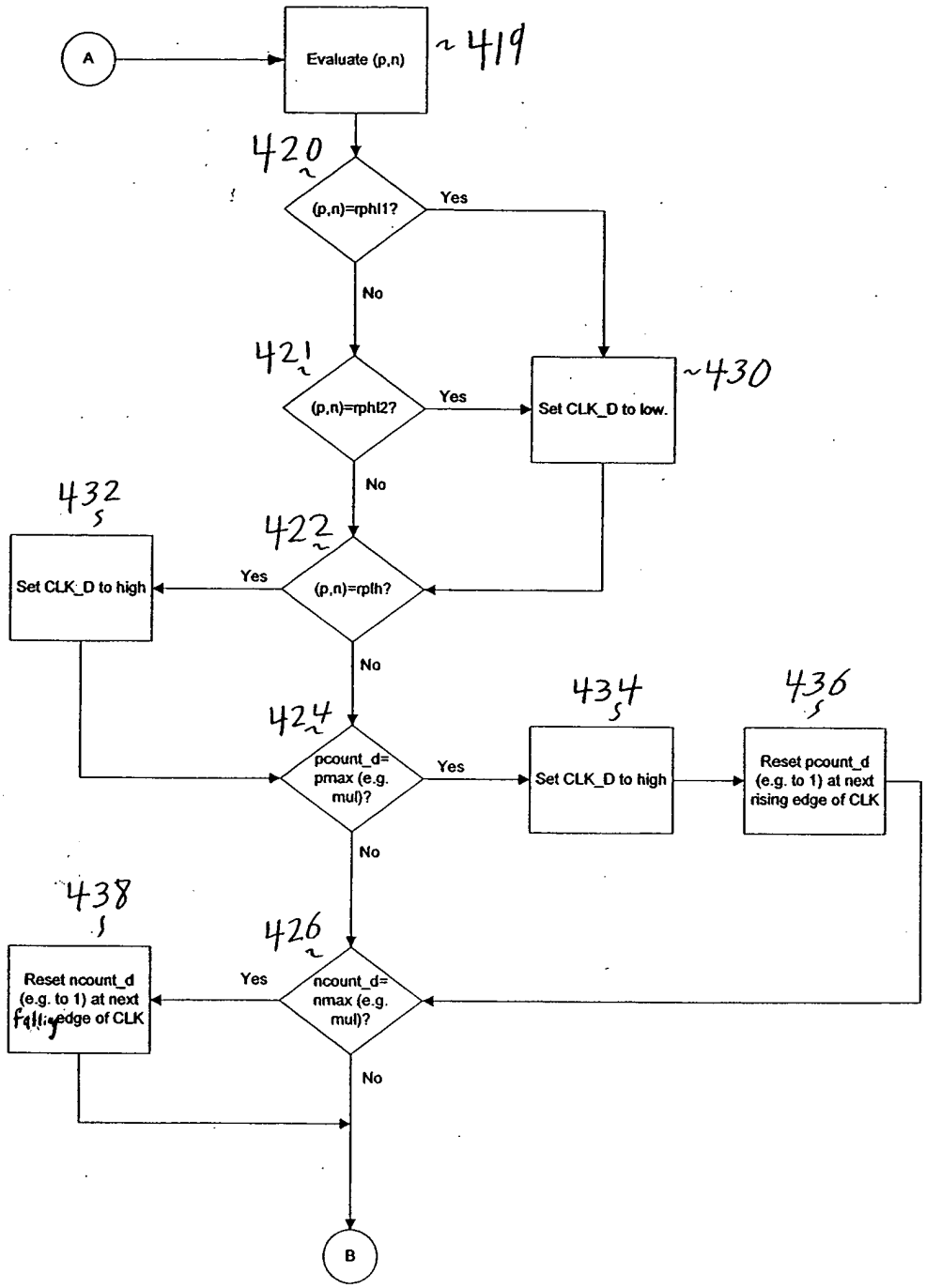
A
Evaluate (p,n)
419
420
(p,n)=rphl1?
Yes
No
421
(p,n)=rphl2?
Yes
Set CLK_D to low.
430
No
432
Set CLK_D to high
422
(p,n)=rpth?
Yes
No
434
436
424
pcount_d= pmax (e.g. mul)?
Yes
Set CLK_D to high
Reset pcount_d (e.g. to 1) at next rising edge of CLK
No
438
426
Reset ncount_d (e.g. to 1) at next falling edge of CLK
Yes
ncount_d= nmax (e.g. mul)?
No
B

FIG. 4B

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